

FORM PTO1449  
(REV. 8-83)DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
11587-10187-39C USSERIAL NO.  
09/657,482

## INFORMATION DISCLOSURE STATEMENT

Use several sheets if necessary)

## APPLICANT

Eliyahou Harari et al.

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## GROUP

2131

## U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>WJH</i>	A1	4 2 8 1 3 9 8	1/1981	McKenny et al.			
<i>WJH</i>	A2	4 6 1 7 6 5 1	10/1986	Ip et al.			
<i>WJH</i>	A3	5 0 4 3 9 4 0	8/1991	Harari			
<i>Duplicate</i>	A4	5 2 9 7 1 4 8	1994	Harari et al.			
<i>WJH</i>	A5	4 4 9 3 0 7 5	1/1985	Anderson et al.			
<i>WJH</i>	A6	4 7 9 6 2 3 3	1/1989	Awaya et al.			
<i>WJH</i>	A7	4 9 1 4 5 2 9	4/1990	Bonke			
<i>WJH</i>	A8	4 0 5 1 3 5 4	9/1977	Choate			
<i>Duplicate</i>	A9	4 7 5 7 4 7 4	1988	Fukushi et al.			

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		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
<i>WJH</i>	B1	0 0 8 6 8 8 6	8/1983	European Patent Appln			
<i>WJH</i>	B2	2 1 3 6 9 9 2	9/1984	UK Patent Appln.			
<i>WJH</i>	B3	0 2 2 0 7 1 8	5/1987	European Patent Appln.			
<i>WJH</i>	B4	0 2 4 3 5 0 3	1/1987	European Patent Appln.			
<i>WJH</i>	B5	0 3 0 0 2 6 4	1/1989	European Patent Appln.			
<i>WJH</i>	B6	A 5 5 7 7 2 3	1/1987	AU Patent			
<i>WJH</i>	B7	WO 8 4 0 0 6 2 8	2/1984	PCT W.I.P.O.			

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

<i>WJH</i>	C1	Wilson, "1-Mbit flash memories seek their role in system design," <u>Computer Design</u> , Vol. 28, No. 5, pps. 30-32 (March 1989)
<i>WJH</i>	C2	Miller, "Semidisk Disk Emulator," <u>INTERFACE AGE</u> , p. 102, November 1982
<i>WJH</i>	C3	Clewitt, "Bubble Memories as a Floppy Disk Replacement," <u>1978 MIDCON Technical Papers</u> , Vol. 2, pp. 1-7, (December 1978)

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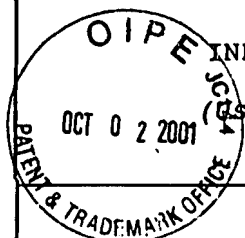
*Lyn V. Hua*

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*These are in parent applications*

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<i>WJH</i>	A10	4	7	3	3	3	9	4		3/1988	Giebel			
<i>WJH</i>	A11	4	5	1	4	8	3	0		4/1985	Hagiwara et al.			
<i>WJH</i>	A12	4	7	9	4	5	6	8		2/1988	Lim et al.			
<i>WJH</i>	A13	4	6	1	2	6	4	0		9/1986	Mehrotra et al.			
<i>WJH</i>	A14	4	5	2	7	2	5	1		2/1985	Nibby, Jr. et al.			
<i>WJH</i>	A15	4	7	4	6	9	9	8		5/1988	Robinson et al.			
<i>WJH</i>	A16	4	9	4	2	5	5	6		2/1990	Sasaki et al.			
<i>WJH</i>	A17	4	7	7	4	7	0	0		9/1988	Satoh et al.			
<i>WJH</i>	A18	4	4	0	5	9	5	2		9/1983	Slakmon			

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<i>WJH</i>	B8	A0	1	0	5	4	5	4	3	3/1989	Japanese Patent Abstr.			
<i>WJH</i>	B9	A0	1	7	8	5	6	4		2/1986	Japanese Patent Abstr.			
<i>WJH</i>	B10	58	-	2	1	5	7	9	4	2/1983	Japan			YES
<i>WJH</i>	B11	58	-	2	1	5	7	9	5	2/1983	Japan			YES
<i>WJH</i>	B12	59	-	1	6	2	6	9	5	3/1984	Japan			YES
<i>WJH</i>	B13	60	-	2	1	2	9	0	0	10/1985	Japan			YES
<i>WJH</i>	B14	62	-	2	8	3	4	9	6	12/1987	Japan			YES

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

<i>WJH</i>	C4	Hancock, "Architecting a CCD Replacement for the IBM 2305 Fixed Head Disk Drive," Digest of Papers, <u>Eighteenth IEEE Computer Society International Conference</u> , pp. 182-184, 1979
<i>WJH</i>	C5	Lucero et al., "A 16 Kbit Smart 5 V-only EEPROM with Redundancy," <u>IEEE Journal of Solid-State Circuits</u> , vol. SC-18, no. 5, pps. 539-543 (October 1983)
<i>WJH</i>	C6	Torelli et al., "An improved method for programming a word-erasable EEPROM," <u>Alta Frequenza</u> , vol. 52, no. 6, pps. 487-494 (Nov.-Dec. 1983)

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<i>Red</i>	A19 4 6 7 2 2 4 0	1987	Smith et al.			
<i>Duplicate</i>	<del>A20 4 6 8 8 2 1 9</del>	<del>1987</del>	<del>Takemao</del>			
<i>Red</i>	A21 4 2 5 0 5 7 0	1981	Tsang et al.			
<i>Red</i>	A22 4 6 0 1 0 3 1	1986	Walker et al.			
<i>Red</i>	A23 4 3 5 5 3 7 6	1982	Gould			
<i>Red</i>	A24 3 6 3 3 1 7 5	1972	Harper			
<i>Red</i>	A25 4 4 9 8 1 4 6	1985	Martinez			
<i>Red</i>	A26 4 9 2 4 3 3 1	1990	Robinson et al.			
<i>Red</i>	A27 4 4 7 9 2 1 4	1984	Ryan			
<i>Red</i>	A28 4 9 5 3 1 2 2	1990	Williams			
<i>Duplicate</i>	<del>A29 4 9 4 9 3 0 9</del>	<del>1990</del>	<del>Rao</del>			

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DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
B15 60 - 0 7 6 0 9 7	1985	Japan			Abstr.
B16 59 - 4 5 6 9 5	1984	Japan			Abstr.
B17 61 - 9 6 5 9 8	1986	Japan			Abstr.
B18 62 - 2 8 3 4 9 7	1987	Japan			Abstr.
B19 63 - 1 8 3 7 0 0	1988	Japan			Abstr.

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

<i>Red</i>	C7	Data Sheet: "27F256 256K(32K x 8) CMOS Flash Memory," <u>Intel Corporation</u> , pps. 1-24 (May 1988)
<i>Red</i>	C8	Preliminary Data Sheet, "48F512 512K Flash EEPROM," <u>SEEQ Technology, Incorporated</u> , pps. 2-1 thru 2-12 (October 1988)
<i>Red</i>	C9	Advanced Data Sheet, "48F010 1024K Flash EEPROM," <u>SEEQ Technology, Incorporated</u> , pps. 2-13 thru 2-24 (October 1988)

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<i>Lu H</i>	A30 4 9 2 0 5 1 8	4/1990	Nakamura et al.			
	A31 4 3 8 0 0 6 6	4/1983	Spencer et al.			
	A32 4 5 2 5 8 3 9	2/1985	Nozawa et al.			
	A33 4 4 6 3 4 5 0	2/1984	Hausele			
	A34 4 3 5 4 2 5 3	12/1982	Naden			
	A35 4 4 2 2 1 6 1	12/1983	Kressel et al.			
	A36 4 4 5 0 5 5 9	5/1984	Bond et al.			
	A37 4 6 5 4 8 4 7	3/1987	Dutton			
<i>Duplicate</i>	<del>A38 4 7 3 3 3 9 4</del>	<del>1988</del>	<del>Durkhard</del>			
<i>Lu H</i>	A39 4 8 9 6 2 6 2	1/1990	Wayama et al.			
	A40 4 9 4 5 5 3 5	2/1990	Hosotani et al.			
	A41 4 2 9 5 2 0 5	10/1981	Kunststadt			
	A42 4 6 1 7 6 2 4	10/1986	Goodman			
	A43 4 2 1 0 9 5 9	7/1980	Wozniak			
	A44 4 6 4 2 7 5 9	2/1987	Foster			
	A45 4 4 5 6 9 7 1	6/1984	Fukuda et al.			
	A46 5 2 2 6 1 6 8	2/1993	Kobayashi et al.			
	A47 4 0 9 3 9 8 5	6/1978	Das			
	A48 4 2 7 9 0 2 4	2/1981	Schrenk			
<i>Lu H</i>	A49 4 6 1 6 3 1 1	10/1986	Sato			

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<i>Lu H</i>	C10	Lai, Robert S., "Writing MS-DOS Device Drivers," The Waite Group, Inc. September 1987, pp. i-xi and 235-319
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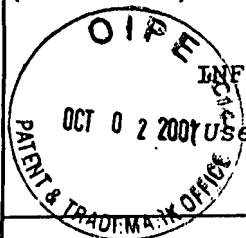
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<i>SwH</i>	A50	4 7 1 8 0 4 1	✓ 1988	Baglee et al.			
	A51	4 7 8 5 4 2 5	✓ 1988	Lavelle			
	A52	4 8 0 0 5 2 0	✓ 1989	Iijima			
	A53	4 8 8 7 2 3 4	✓ 1989	Iijima			
	A54	4 9 4 9 2 4 0	✓ 1990	Iijima			
	A55	5 0 5 3 9 9 0	✓ 1991	Kreifels et al.			
<i>Duplicate SwH</i>	<del>A56</del>	<del>5 0 7 0 4 7 4</del>	<del>1991</del>	<del>Tuma et al.</del>			
	A57	5 0 9 5 3 4 4	✓ 1992	Harari			
<i>Duplicate</i>	<del>A58</del>	<del>5 6 0 2 9 8 7</del>	<del>1997</del>	<del>Harari et al.</del>			

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## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)


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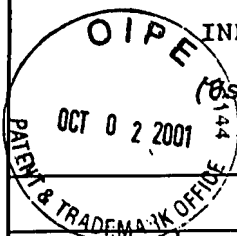
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<i>LSH</i>	A59 4 2 7 2 8 3 0	6/9/81	Moench			
	A60 4 2 8 7 5 7 0	9/1/81	Stark			
	A61 4 5 8 6 1 6 3	4/29/86	Koike			
	A62 4 6 5 3 0 2 3	3/24/87	Suzuki et al.			
	A63 4 8 4 7 8 0 8	7/11/89	Kobatake			
	A64 4 8 9 9 2 7 4	2/6/90	Hansen et al.			
<i>LSH</i>	A65 4 9 5 8 3 1 5	9/18/90	Balch			

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<i>LSH</i> B20 2 2 0 2 3 4 9	2/1988	UK Patent Appln.			
B21 3 8 1 2 1 4 7	5/1988	Deutschland			
B22 0 2 8 4 9 8 1	7/1988	European Patent Appln.			
<i>LSH</i> B23 61 - 2 5 2 2 9	4/1986	Japanese Patent Appln.			

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<i>LSH</i> C11	Stark, M., "Two Bits Per Cell Rom," IEEE Catalog No. 81-CH1626-1, Library of Congress No. 80-85186, Order No. 341, Spring Comp Con 1981, Feb. 23-26, Twenty-Second Computer Society International Conference, San Francisco, CA
C12	Furuyama et al., "An Experimental 2-Bit/Cell Storage Dram For Macro Cell Or Memory-On-Logic Application," pp. 4.4.1 - 4.4.4, IEEE, (1988)
C13	Horiguchi et al., "An Experimental Large-Capacity Semiconductor File Memory Using 16-Levels Cell Storage," IEEE Journal Of Solid-State Circuits, Vol. 23, No. 1, February 1988
C14	Krick, P.J., "Three-State MNOS Fet Memory Array," IBM Technical Disclosure Bulletin, Vol. 18, No. 12, pps. 4192-4193 (May, 1976)
C15	Alberts, et al., "Multi-Bit Storage Fet EAROM Cell," IBM Technical Disclosure Bulletin, Vol. 24, No. 7A, pps. 3311-3314 (December, 1981)
<i>LSH</i> C16	Bleiker et al., "A Four-State EEPROM Using Floating-Gate Memory Cells," IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 3 (June, 1987)

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<i>RKH</i>	A66 4 7 2 7 5 1 2	2/23/88	Birkner et al.			
	A67 4 7 9 7 5 4 3	1/10/89	Watanabe			
	A68 4 7 9 8 9 4 1	1/17/89	Watanabe			
	A69 4 8 2 9 1 6 9	5/9/89	Watanabe			
	A70 4 8 3 1 2 4 5	5/16/89	Ogāsawara			
	A71 4 8 5 3 5 2 2	8/1/89	Ogasawara			
	A72 4 8 9 1 5 0 6	1/2/90	Yoshimatsu			
<i>RKH</i>	A73 5 3 5 9 7 2 6	10/25/94	Thomas			

## FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
B24 2 1 7 2 1 2 6	10/1986	UK Patent Appln.			

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)


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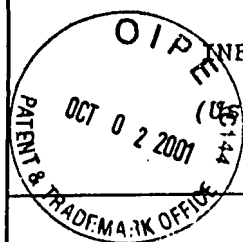
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<i>RLH</i>	A74	3 3 3 1 0 5 8	7/11/67	Perkins			
	A75	3 4 4 2 4 0 2	5/6/69	Baxter			
	A76	3 6 9 3 1 5 9	9/19/72	Hilberg			
	A77	3 7 3 5 3 6 8	5/22/73	Beausoleil			
	A78	3 7 5 3 2 4 4	8/14/73	Sumilas et al.			
	A79	3 7 6 5 0 0 1	9/9/73	Beausoleil			
	A80	3 7 7 2 6 5 2	11/13/73	Hilberg			
	A81	3 7 8 1 8 2 6	12/25/73	Beausoleil			
	A82	3 8 0 0 2 9 4	3/26/74	Lawlor			
	A83	3 9 5 5 1 8 0	5/4/76	Hirtle			
<i>RLH</i>	A84	4 0 7 4 2 3 6	2/14/78	Ishida			

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<i>RLH</i>	B25	59 - 1 5 4 5 2 5	3/1984	Japan			Abstract
	B26	63 - 1 3 8 4 8 3	6/1988	Japan			Abstract
	B27	63 - 1 8 4 8 8 9	7/1988	Japan			Abstract
	B28	64 - 0 5 9 4 8 6	3/1989	Japan			Abstract
<i>RLH</i>	B29	64 - 0 7 0 8 4 3	3/1989	Japan			Abstract

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<i>RLH</i>	C17	"Nonvolatility" Semiconductor vs. Magnetic," IEEE (reprint), International Solid-State Circuits Conference, February 17-19, 1998, Richard Pashley, Organizer/Moderator, p. 6-393.
<i>RLH</i>	C18	"High-Density Flash EEPROMS are about to Burst on the Memory Market", Electornics, March 3, 1988, J. Robert Lineback.
<i>RLH</i>	C19	"Erasable/Programmable solid state memories", EDN, November 14, 1985, Denny Cormier, Western Editor, pp. 145-153.

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<i>lvh</i>	A85 4 2 1 4 2 8 0	7/22/80	Halfhill et al.			
	A86 4 2 1 8 7 4 2	8/19/80	Carlton et al.			
	A87 4 2 7 7 8 2 7	7/7/81	Carlson et al.			
<i>Duplicate</i>	<del>A88 4 2 9 5 2 0 5</del>	<del>10/13/81</del>	<del>Kunstedt</del>			
	A89 4 3 1 0 9 0 1	1/12/82	Harding et al.			
	A90 4 3 1 9 3 2 3	3/9/82	Ermolovich et al.			
	A91 4 3 9 8 2 4 8	8/9/83	Hsia et al			
	A92 4 4 2 6 6 8 8	1/17/84	Moxley			
	A93 4 4 4 3 8 4 5	4/17/84	Hamilton et al.			
	A94 4 4 6 7 4 2 1	8/21/84	White			
<i>lvh</i>	A95 4 4 9 5 5 7 2	1/22/85	Bosen			

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<i>lvh</i> B30 0 0 0 6 5 5 0	1980	EP			

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<i>lvh</i>	C20	"A Reconfigurable Interconnect for In-Silicon Electronic Assembly", 32nd Electronic Components Conference, May 10-12, 1982, Hsia et al., pp. 7-16.
<i>lvh</i>	C21	"Adaptive Wafer Scale Integration", Japanese Journal of Applied Physics, vol. 19, supp. 19-1, 1980, Yukun Hsia et al., pp. 193-202.
<i>lvh</i>	C22	"Nonvolatile Memories: A 5V-Only 256k Bit CMOS Flash EEPROM", 1989 IEEE International Solid State Circuits Conference, No. 0193-6530/89/0000-0132, February 16, 1989, D'Arrigo et al, pp. 132-133.

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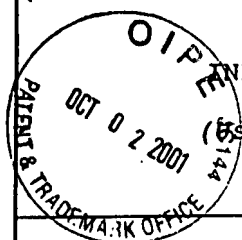
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<i>LuH</i>	A96	4	5	0	6	3	2	4		3/19/85	Healy			
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	A98	4	5	7	3	1	4	1		2/25/86	Simon			
	A99	4	5	7	8	7	7	4		3/25/86	Muller			
	AA1	4	5	8	4	6	8	1		4/22/86	Singh et al			
	AA2	4	6	3	0	2	3	0		12/16/86	Sundet			
	AA3	4	6	3	8	4	6	5		1/20/87	Rosini et al.			
	AA4	4	6	4	4	4	9	4		2/17/87	Muller			
	AA5	4	6	4	8	0	7	6		3/3/87	Schrenk			
	AA6	4	6	5	4	8	2	9		3/31/87	Jiang et al.			
<i>LuH</i>	AA7	4	6	8	0	7	3	6		7/14/87	Schrenk			

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	AA9 4 7 1 3 7 5 6	12/15/87	Mackiewicz et al.			
	AB1 4 7 3 3 3 7 5	3/22/88	Terashima			
	AB2 4 7 3 7 9 3 5	4/12/88	Wawersig et al.			
	AB3 4 7 4 4 0 6 2	5/10/88	Nakamura et al.			
	AB4 4 7 4 8 3 2 0	5/31/88	Yorimoto et al.			
	AB5 4 7 5 0 1 5 8	6/7/88	Giebel et al.			
	AB6 4 7 5 1 7 0 3	6/14/88	Picon et al.			
	AB7 4 7 8 0 8 5 5	10/25/88	Iida et al.			
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	AC2	4	7	9	1	6	1	5		12/13/88	Pelley III et al.			
	AC3	4	8	0	3	5	5	4		2/7/89	Pape			
	AC4	4	8	1	7	0	0	2		3/28/89	Sansone et al.			
	AC5	4	8	5	3	8	5	3		8/1/89	Yamamura et al.			
	AC6	4	9	3	1	9	4	3		6/5/90	Vermesse			
	AC7	4	9	3	9	5	9	8		7/3/90	Kulakowski et al.			
	AC8	4	9	6	4	0	7	4		10/16/90	Suzuki et al.			
	AC9	4	9	7	7	5	0	3		12/11/90	Rudnick et al.			
	AD1	4	9	8	4	1	9	1		1/8/91	Vermesse			
<i>SW</i>	AD2	5	1	4	6	5	7	1		9/8/92	Logan			

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	AD5	5	2	2	6	1	3	6		7/6/93	Nakagawa			
	AD6	5	2	3	9	6	6	2		8/24/93	Danielson et al.			
	AD6	5	2	5	3	3	5	0		10/12/93	Foster et al.			
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	AD9	3 8 8 2 4 7 0	5/6/75	Hunter			
	AE1	4 0 5 1 4 6 0	9/27/77	Yamada et al.			
	AE2	4 4 3 4 4 8 7	2/28/84	Rubinson et al.			
	AE3	4 4 7 5 1 9 4	10/2/84	LaVallee et al.			
	AE4	4 7 6 8 1 9 3	8/30/88	Takemae			
<i>Lu</i>	AE5	5 2 2 2 0 4 6	6/22/93	Kreifels et al.			

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<i>Lu</i>	C19	"MS-DOS Developer's Guide", Angermeyer et al., 1986, The Waite Group, Inc., p. 287.

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<i>lvh</i>	AE8 4 7 4 2 2 1 5	5/3/88	Daughters et al.			
<i>Duplicate lvh</i>	<del>AE9 4 7 6 8 1 9 3</del>	<del>8/30/88</del>	<del>Takemae</del>			
<i>lvh</i>	AF1 4 8 6 2 2 0 0	8/29/89	Hicks			
<i>lvh</i>	AF2 5 0 9 3 7 3 1	3/3/92	Watanabe et al.			
<i>lvh</i>	AF3 5 1 0 1 2 4 9	3/31/92	Hijiya et al.			
<i>Duplicate lvh</i>	<del>AF4 5 2 2 2 0 4 6</del>	<del>6/22/93</del>	<del>Kreifels et al.</del>			

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<i>/</i>	C48	Cacharelis, et al., "A Single Transistor Electrically Alterable Cell", IEEE Electron Device Letters, Vol. EDL-6, No. 10, October 1985, pg. 519-521.
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(Use several sheets if necessary)						Eliyahou Harari et al.			
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LoH	AS	5,936,971	Aug. 1999	Harari et al.					
Foreign Patent Documents									
								Translation	
		Document	Date	Country	Class	Subclass	Yes	No	
	AT								
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)									
LoH	AU	Intel Corporation, 27F256, 256K (32Kx8) CMOS Flash Memory, May 1988, pp. 1-21.							
Examiner		Date Considered							
Py V. Hua		2/27/02							
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.									